PTO-2055-B (Rev. 10/03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE

In re Patent No.: 6,535,780

Patentee: Anderson, George, et al.

Patent Date: March 18, 2003

Application No.: 09/471,675

Filing Date: December 24, 1999

Direct to:

Mail Stop RECONSTRUCTION
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

NOTICE UNDER 37 CFR 1.251 - Patent

Statement (check the appropriate box):

☐ The copy submitted with this reply is a complete and accurate copy of applicant's record of all of the correspondence between the Office and the applicant for the above-identified application (except for U.S. patent documents), and applicant is not aware of any correspondence between the Office and applicant for the above-identified application that is not among applicant's records.

☐ The copy of the paper(s) listed in the notice under 37 CFR 1.251 is/are a complete and accurate copy of applicant's record of such paper(s).

☑ The papers produced by applicant are applicant's complete record of all of the correspondence between the Office and the applicant for the above-identified application (except for U.S. patent documents), and applicant is not aware of any correspondence between the Office and the applicant for the above-identified application that is not among applicant's records.

☐ Applicant does not possess any record of the correspondence between the Office and the applicant for the above-identified application.

January 29, 2010
Date

Signature

Travis R. Henderson
Typed or printed name

A copy of this notice should be returned with the reply.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Customer Num: 000000

THE LAW OFFICES OF MIKIO ISHIMARU
333 W. EL CAMINO REAL
SUITE 330
SUNNYVALE CA 94087

MAINTENANCE FEE STATEMENT

The data shown below is from the records of the U.S. Patent and Trademark Office. If the maintenance fee and any necessary surcharge have been timely paid for the patent listed below, the notation "PAID" will appear in the "STAT" column.

If the statement of small entity status is defective the reason will be indicated below in the "Small Entity" status column. THE STATEMENT OF SMALL ENTITY STATUS WILL BE ENTERED UPON RECEIPT OF ACCEPTABLE CORRECTION.

PATENT NUMBER	FEE AMT	SUR CHARGE	U.S. APPLICATION NUMBER	PATENT ISSUE DATE	APPL. FILING DATE	PAYMENT YEAR	SMALL ENTITY?	STAT	ATTY DKT NUMBER
6,535,780	**$450.00**	**$0.00**	**09/471,675**	**03/18/03**	**12/24/99**	**04**	**YES**	**PAID**	**1015-003**

Direct any questions about this notice to:
Mail Stop M Correspondence
Director of the U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Docket Number: 1015-003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number	6,535,780 B1
Issued	3/18/2003
Name of Patentee	George Leland Anderson
Title of Invention	HIGH SPEED PROGRAMMER SYSTEM

Commissioner for Patents
Washington, D.C. 20231
ATTENTION: Decision and Certificate of Correction
Branch of the Patent Issue Division

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT

Please issue a Certificate of Correction for the following mistakes in the above-referenced patent.

☒ **FOR PTO MISTAKE (37 C.F.R. § 1.322(a))**
The exact page and line number where the errors are shown correctly in the application file are:

1. In the specification, page 4, line 2
2. In the specification, page 9, line 20

The exact column and line number where the error occurs in the Patent are:

1. Column 2, line 10, delete "quipment" and insert therefore --equipment--
2. Column 7, line 13, delete "Shiftinz" and insert therefore --Shifting--

☒ **FOR APPLICANT'S MISTAKE (37 C.F.R. 1.323)**

The exact page and line number where the error occurs in the application are:

3. In the specification, page 6, line 7
4. In the specification, page 7, line 2
5. In the specification, page 10, line 15
6. In the specification, page 10, line 15

The exact column and line number the error occurs in the Patent are:

3. Column 4, line 49, delete "correpsonding" and insert therefore --corresponding--
4. Column 5, line 27, delete "level-shifing" and insert therefore --level-shifting--
5. Column 7, line 50, delete "transferrring" and insert therefore --transferring--
6. Column 7, line 52, delete, "transfering" and insert therefore --transferring--

Patent Number: 6, 535,780 B1
Docket Number: 1015-003 Patent

☒ Attached hereto, in duplicate, is Form PTO-1050, with at least one copy being suitable for printing.

☒ Please send the Certificate to:

Name Mikio Ishimaru

Address The Law Offices of Mikio Ishimaru
1110 Sunnyvale-Saratoga Road, Suite A1
Sunnyvale, CA 94087

☒ Please pay the fee of $ 100.00 as required by 37 CFR 1.20(a), and the fee for ___additional copies of the Certificate of Correction as follows:

☒ Charge Deposit Account 50-0374 the sum of $100.00 plus the charge for copies of ____ the Certificate of Correction. A duplicate of this request is attached.

☒ Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account No. 50-0374 and credit any excess fees to such deposit account.

Mikio Ishimaru

Mikio Ishimaru
Reg. No.: 27,449

March 24, 2003

CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R.1.8a)

I hereby certify that this correspondence is on the date shown below being:

☒ Deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the: Office of Initial Patent Examination's
Customer Service Center
Commissioner for Patents
Washington, D.C. 20231

Date: March 24, 2003

Signature Vickie Ishimaru

Vickie Ishimaru

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	03/18/2003	6535780	1015-003	7801

22898 7590 02/27/2003

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

APPLICANT(S):

GEORGE LELAND ANDERSON, BOTHELL, WA;
ROBIN EDWARD CAMERON, SNOHOMISH, WA;
SCOTT ALLEN FERN, KENT, WA;

TO:Auto-reply fax to 408 738 0881 COMPANY:

Auto-Reply Facsimile Transmission

UNITED STATES PATENT AND TRADEMARK OFFICE

TO: Fax Sender at 408 738 0881

Fax Information
Date Received: 1/28/03 7:15:36 PM [Eastern Standard Time]
Total Pages: 4 (including cover page)

ADVISORY: This is an automatically generated return receipt confirmation of the facsimile transmission received by the Office. Please check to make sure that the number of pages listed as received in Total Pages above matches what was intended to be sent. Applicants are advised to retain this receipt in the unlikely event that proof of this facsimile transmission is necessary. Applicants are also advised to use the certificate of facsimile transmission procedures set forth in 37 CFR 1.8(a) and (b), 37 CFR 1.6(f). Trademark Applicants, also see the Trademark Manual of Examining Procedure (TMEP) section 306 et seq.

Received Cover Page ========>

JAN-28-2003 TUE 04:12 PM LAW OFFICE OF M ISHIMARU FAX NO. 408 738 0881 P. 01

The Law Offices of Mikio Ishimaru
Intellectual Property Law
Patents - Licensing - Strategy - & Related Matters
1110 Sunnyvale-Saratoga Road, Suite A1
Sunnyvale, CA 94087
Telephone: (408) 738-0592
Fax: (408) 738-0881

Fax

To:	Office of Publications Box Issue Fee	From:	Mikio Ishimaru
Fax:	(703) 746-4000	Pages:	4, including this page
Phone:	(703) 305-8283	Date:	January 28, 2003
Re:	U.S. Patent Application Serial No. 09/471,675	CC:	

☒ Issue Fee ☐ Information ☐ Other

IMPORTANT

The information contained in this facsimile is intended only for the use of the individual or entity to whom it is addressed. If you are not the intended recipient, you are hereby notified that any use, dissemination, distribution or copying of this communication is strictly prohibited. If you have received this facsimile in error, please immediately notify us by telephone, and return the original message to us at the address above via the U.S. Postal Service. Thank you.

For confirmation or assistance, call (408) 738-0881.

Dear Publications:

Attached are a Certificate of Transmission and Issue Fee for U.S. Patent Application Serial No. 09/471,675 (attorney docket no. 1015-003).

Respectfully submitted,

Mikio Ishimaru
Reg. No. 27,449

Received from < 408 738 0881 > at 1/28/03 7:15:36 PM [Eastern Standard Time]

P.01

TRANSACTION REPORT

JAN-28-2003 TUE 04:14 PM

FOR: LAW OFFICE OF M ISHIMARU 408 738 0881

DATE	START	RECEIVER	TX TIME	PAGES	TYPE	NOTE	M#	DP
JAN-28	04:12 PM	17037464000	1'56"	4	SEND	OK	157	

TOTAL : 1M 56S PAGES: 4

The Law Offices of Mikio Ishimaru

Intellectual Property Law
Patents - Licensing - Strategy - & Related Matters
1110 Sunnyvale-Saratoga Road, Suite A1
Sunnyvale, CA 94087
Telephone: (408) 738-0592
Fax: (408) 738-0881

Fax

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Re:	U.S. Patent Application Serial No. 09/471,675	CC:	

☒ Issue Fee ☐ Information ☐ Other

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Fax:	(703) 746-4000	Pages:	4, including this page
Phone:	(703) 305-8283	Date:	January 28, 2003
Re:	U.S. Patent Application Serial No. 09/471,675	CC:	

☒ Issue Fee ☐ Information ☐ Other

Dear Publications:

Attached are a Certificate of Transmission and Issue Fee for U.S. Patent Application Serial No. 09/471,675 (attorney docket no. 1015-003).

Respectfully submitted,

Mikio Ishimaru

Mikio Ishimaru
Reg. No. 27,449

PTO/SB/97 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Certificate of Transmission under 37 CFR 1.8

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office

on January 28, 2003
Date

Tamara Tucker
Signature

Tamara Tucker
Typed or printed name of person signing Certificate

Note: Each paper must have its own certificate of transmission, or this certificate must identify each submitted paper.

With reference to serial number 09/471,675, the following are being submitted:

Fax Cover Sheet
Certificate of Transmission
Issue Fee Transmittal

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Box ISSUE FEE
Commissioner for Patents
Washington, D.C. 20231
Fax (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

22898 7590 11/06/2002

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

CERTIFICATE OF TRANSMISSION (Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

TITLE OF INVENTION: HIGH SPEED PROGRAMMER SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	~~$640~~ $650	$0	~~$640~~ $650	02/06/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
HECKLER, THOMAS M	2185	713-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Mikio Ishimaru
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: DATA I/O CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Redmond, WA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

☒ Issue Fee
☐ Publication Fee
☒ Advance Order - # of Copies 2

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-0374 (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) Mikio Ishimaru (Date) 1/28/03
Mikio Ishimaru Reg# 27,449

NOTE; The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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TRANSMIT THIS FORM WITH FEE(S)

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

22898 7590 01/23/2003

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

EXAMINER
HECKLER, THOMAS M

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Second Supplemental **Notice of Allowability**	**Application No.** 09/471,675	**Applicant(s)** ANDERSON ET AL.
	Examiner Thomas Heckler	**Art Unit** 2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *inquiry regarding priority*.
2. ☒ The allowed claim(s) is/are *1-28*.
3. ☒ The drawings filed on *05 December 2002* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☐ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____ .
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
6☐ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☐ Examiner's Statement of Reasons for Allowance
9☐ Other .

Thomas Heckler
Primary Examiner
Art Unit: 2185

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

22898 7590 01/08/2003

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

EXAMINER	
HECKLER, THOMAS M	
ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental **Notice of Allowability**	**Application No.** 09/471,675	**Applicant(s)** ANDERSON ET AL.	
	Examiner Thomas Heckler	**Art Unit** 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *drawing correction of 12/5/02*.
2. ☒ The allowed claim(s) is/are *1-28*.
3. ☒ The drawings filed on *05 December 2002* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

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7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☐ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

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2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____ .
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
6☐ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☐ Examiner's Statement of Reasons for Allowance
9☐ Other

Thomas Heckler
Primary Examiner
Art Unit: 2185

Docket No.: 1015-003

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	George Leland Anderson et al.	: Confirmation No.:	7801
Serial No.:	09/471,675	: Examiner:	Thomas Heckler
Filed:	12/24/1999	: Group Art Unit:	2185
For:	HIGH SPEED PROGRAMMER SYSTEM	:	

OFFICIAL DRAFTSPERSON
Drawing Processing Branch
Washington, D.C. 20231

DRAWING TRANSMITTAL LETTER

Sir/Madam:

Applicants have amended Figs.1, 3, and 4 in compliance with the Examiners request under 35 U.S.C. § 1.83(a) and in compliance with MPEP § 11.11(a), which states:

> "The drawings shall not contain text matter, except a single word or words, when absolutely indispensable, such as "water," "steam," "open," "closed," "section on AB," and, in the case of electric circuits and block schematic or flow sheet diagrams, a few short catch words indispensable for understanding."

The drawings are believed to be allowable and prompt issuance of this application is requested. Enclosed herewith please find:

☒ 3 sheets of redlined drawing(s) which indicate the examiners changes to the drawing(s) Figs. 1, 3, and 4.

☒ 4 sheets of corrected formal drawing(s).

I hereby certify that, on the date shown below, this correspondence is being deposited with the United States Postal Service with sufficient postage as:

☐ First Class Mail

☒ "Express Mail Post Office to Addressee" service under 37 CFR 1.10

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in an envelope addressed to: Commissioner for Patents
Box Issue Fee
Washington, D.C. 20231

Date of Deposit: December 5, 2002

Signature: Vickie Ishimaru
Vickie Ishimaru

Respectfully submitted,

Mikio Ishimaru
Reg. No. 27,449

Date: December 5, 2002

1110 Sunnyvale-Saratoga Rd., Ste. A1
Sunnyvale, CA 94087
Tel: (408) 738-0592
Fax: (408) 738-0881

Title: HIGH SPEED PROGRAMMER SYSTE
Inventors: George Leland Anderson, et al.
Docket No.: 1015-003
Contact: Mikio Ishimaru (408) 738-0592

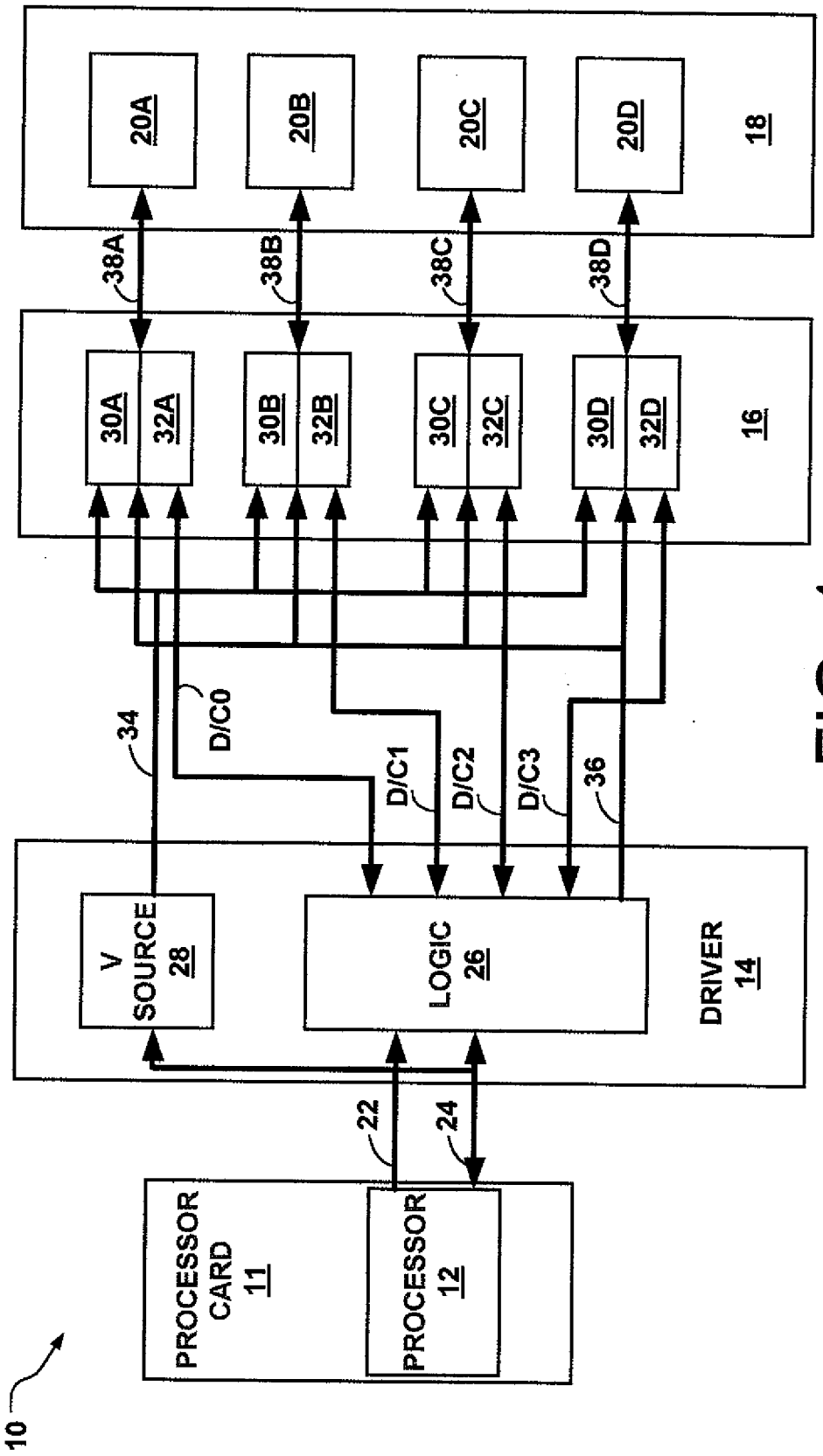

FIG. 1

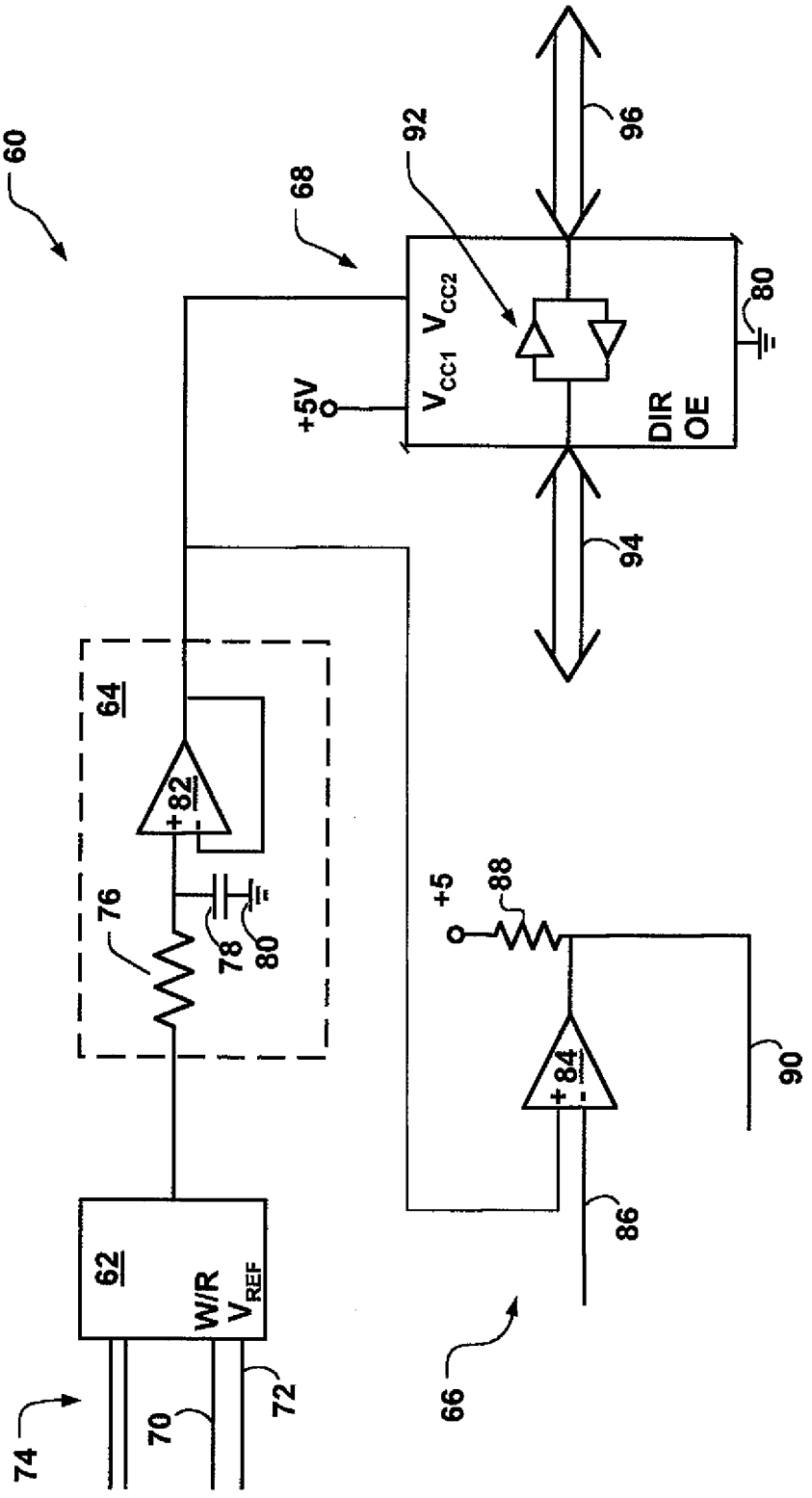
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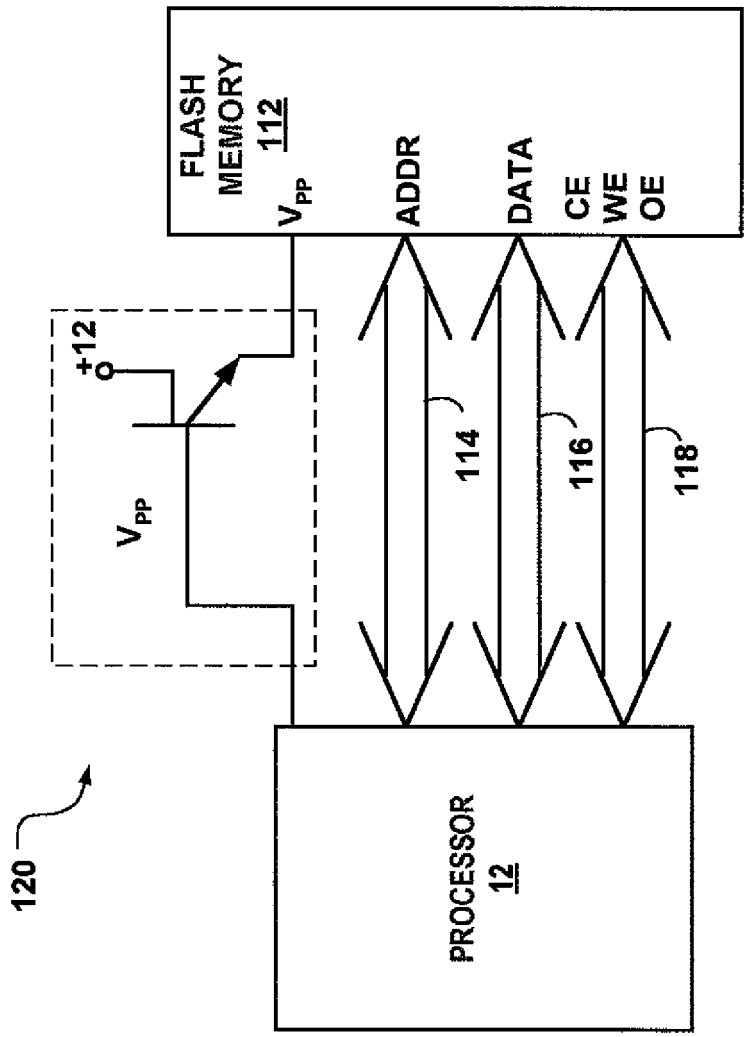
FIG. 2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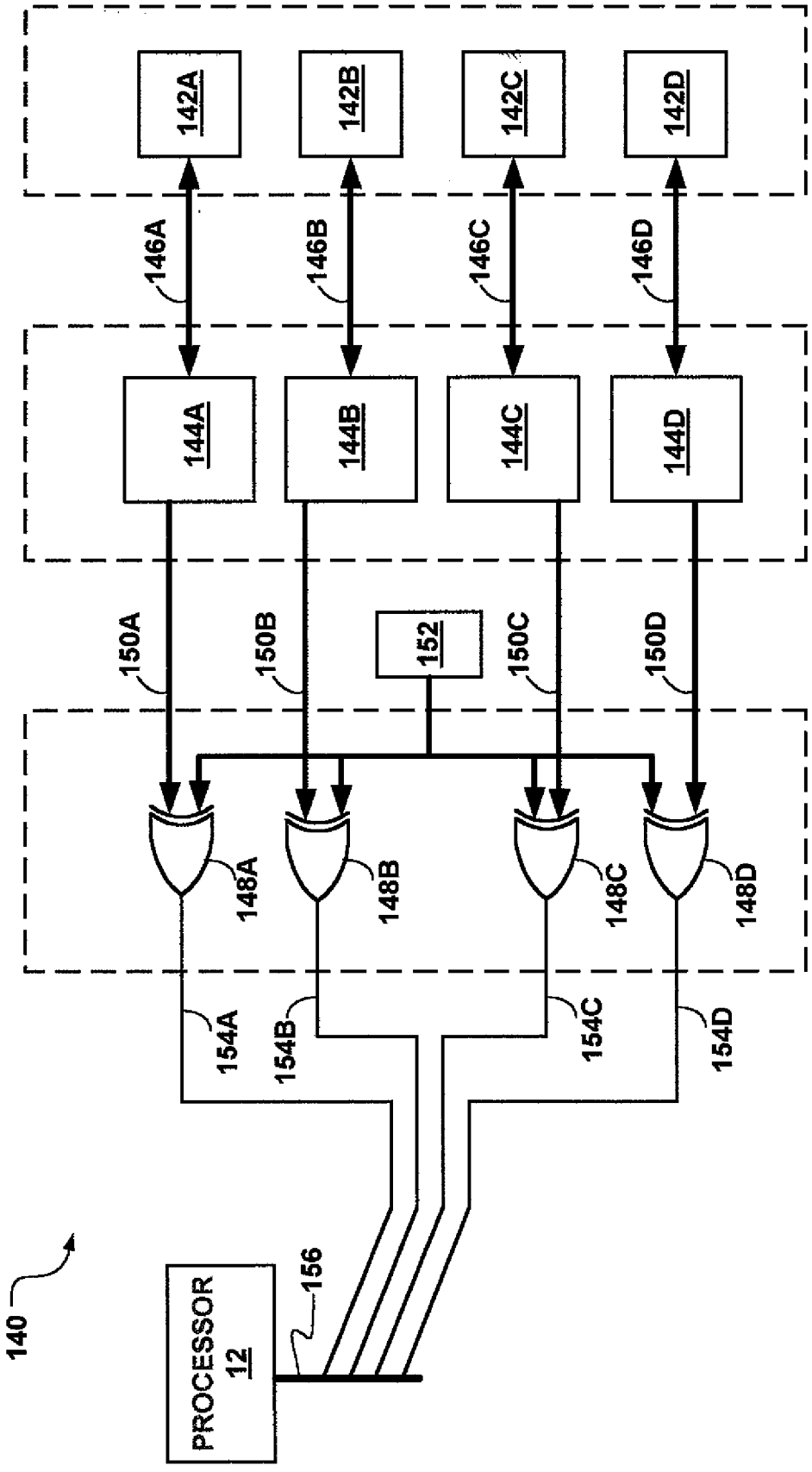
PROCESSOR 12

FIG. 3


142A
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150C
150D
148A
148B
148C
148D
154A
154B
154C
154D
156
PROCESSOR 12
140

FIG. 4

The Law Offices of Mikio Ishimaru

Intellectual Property Law
Patents - Licensing - Strategy - & Related Matters
1110 Sunnyvale-Saratoga Road, Suite A1
Sunnyvale, CA 94087
Telephone: (408) 738- 0592
Fax: (408) 738-0881

Fax

To:	Examiner Thomas M. Heckler Customer Service Group Art Unit 2100	From:	Mikio Ishimaru
Fax:	703-746-7239	Pages:	2
Phone:	703-305-3900	Date:	November 13, 2002
Re:	U.S. Patent Application Serial No. 09/471,675	CC:	Attorney Docket Number: 1015-003

☒ Request for Supplemental Notice of Allowabilty

Dear Examiner Heckler:

Enclosed is a copy of the Notice of Allowance for U.S. Patent Application Serial No. 09/471,675 (attorney docket no. 1015-003). Please acknowledge domestic priority by checking box number 5, which claims priority from the provisional application U.S. Provisional Application Serial No.: 60/164,782 (attorney docket no.: 1015-003P).

Respectfully submitted,

Mikio Ishimaru

Mikio Ishimaru
Reg. No. 27,449

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22898 7590 11/06/2002

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

MIKIO ISHIMARU
NOV 12 2002
RECEIVED

EXAMINER	
HECKLER, THOMAS M	
ART UNIT	CLASS-SUBCLASS
2185	713-001000

DATE MAILED: 11/06/2002

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

TITLE OF INVENTION: HIGH SPEED PROGRAMMER SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$640	$0	$640	02/06/2003

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (REV. 04-02) Approved for use through 01/31/2004.

Notice of Allowability	Application No.	Applicant(s)	
	09/471,675	ANDERSON ET AL.	
	Examiner	Art Unit	
	Thomas Heckler	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
2. ☒ The allowed claim(s) is/are *1-28*.
3. ☒ The drawings filed on *24 December 1999* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☒ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☒ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____ .
5☒ Information Disclosure Statements (PTO-1449), Paper No. *2-4*.
6☒ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other

Thomas Heckler
Primary Examiner
Art Unit: 2185

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

22898 7590 11/06/2002

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087
UNITED STATES

EXAMINER	
HECKLER, THOMAS M	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/06/2002

Determination of Patent Term Extension under 35 U.S.C. 154 (b)
(application filed after June 7, 1995 but prior to May 29, 2000)

The patent term extension is 0 days. Any patent to issue from the above identified application will include an indication of the 0 day extension on the front page.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date that determines patent term extension is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system. (http://pair.uspto.gov)

Any questions regarding the patent term extension or adjustment determination should be directed to the Office of Patent Legal Administration at (703)305-1383.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

22898 7590 11/06/2002

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087
UNITED STATES

EXAMINER	
HECKLER, THOMAS M	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/06/2002

Notice of Possible Fee Increase on October 1, 2002

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2002, then the amount due may be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there may be an increase in fees effective on October 1, 2002. See Revision of Patent and Trademark Fees for Fiscal Year 2003; Notice of Proposed Rulemaking, 67 Fed. Reg. 30634, 30636 (May 7, 2002). Although a change to the amount of the publication fee is not currently proposed for October 2002, if the issue fee or publication fee is to be paid on or after October 1, 2002, applicant should check the USPTO web site for the current fees before submitting the payment. The USPTO Internet address for the fee schedule is: http://www.uspto.gov/main/howtofees.htm.

If the issue fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due," but not the correct amount in view of any fee increase, a "Notice to Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice to Pay Balance of Issue Fee," if the response to the Notice of Allowance and Fee(s) due form is to be filed on or after October 1, 2002 (or mailed with a certificate of mailing on or after October 1, 2002), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

1. The following changes to the drawings are required by the examiner: labels are required for the boxes of Figs. 1, 3, 4 as per 37 C.F.R. 1.83(a). In order to avoid abandonment of the application, applicant must make these drawing changes.

2. The following is an examiner's statement of reasons for allowance: the prior art does not teach a processing mechanism for processing unprocessed micro devices into processed micro devices comprising a pin driver module for routing address, data and control signals to a backplane module and provide a first plurality of voltages to the backplane module, the backplane module routing the address, data and control signals and providing a second plurality of voltages to at least one socket wherein the unprocessed micro device is placed;

nor does the prior art teach a buffer circuit for a processing mechanism capable of processing unprocessed micro devices into processed micro devices comprising a digital-to-analog converter to generate a first variable DC voltage, an amplifier responsive to the DC voltage to generate a second variable DC voltage, and a level-shifting translating buffer for transferring data signals from a processor to the unprocessed micro devices and for transferring the device data signals from the processed micro devices to the processor, the buffer responsive to a voltage and the second variable DC voltage to provide a plurality of logic levels for the device data signals;

nor does the prior art teach a method for programming a programmable micro device comprising providing a first address from a processor, providing a first data corresponding to the

first address, and providing a control signal to enable the micro device to accept the data at a memory location identified by the first address;

nor does the prior art teach a method for reading a programmable micro device comprising providing a first address from a processor to the micro device and providing a control signal from the processor to the micro device to enable the device to provide a first data from a memory location identified by the first address;

nor does the prior art teach a programming mechanism capable of programming unprogrammed micro devices into programmed micro devices comprising a plurality of sockets for placement of processed micro devices, a plurality of data buffer/registers, each coupled to a socket for receiving a first data, a plurality of compare circuits having one input coupled to a respective buffer/register, an expected data register coupled to the second input of a respective compare circuit, and a processor coupled to the output of each of the plurality of compare circuits, wherein each compare circuit provides a first logic level when the first data matches the first expected data, and provides a second logic level when the first data does not match the first expected data;

nor does the prior art teach a method for verifying data programmed in a plurality of programmed micro devices comprising providing to each of a plurality of data buffer/registers a first data stored in each of the plurality of programmed micro devices, providing the first data to a first input of a plurality of compare circuits, providing a first expected data from an expected data register to a second input of each of the plurality of compare circuits, comparing the first data

with the first expected data, outputting a first logic level from one of the compare circuits when the first data matches with the first expected data, and outputting a second logic level from one of the compare circuits when the first data does not match with the first expected data.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom Heckler whose telephone number is (703) 305-9666.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (703) 305-3900.

THOMAS M. HECKLER
PRIMARY EXAMINER

TH
November 5, 2002

FORM PTO-1449

Docket No.:	Serial No.:
1015-003	09/471,675
Applicant: George Leland Anderson et al.	
Filing Date: December 24, 1999	Group: 2185

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

REFERENCE DESIGNATION — U. S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass
	1A					
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Name	Class	Subclass	Translation	
							Yes	No
	1L							
	1M							
	1N							
	1O							
	1P							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	1R	BP-6500 In-Line Programming System brochure, BP Microsystems, Inc. 1999, 2 pages.
	1S	BP-6500 In-Line Programming System Data Sheet, BP Microsystems, Inc. 1999, 1 page.
	1T	"BP-6500 In-Line Programming & Fifth Generation Technology", BP Microsystems, Inc. 1999, 7 pages.

Examiner Thomas Lee — Date Considered 11-5-02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

FORM PTO-1449

OIPE 3700 NOV 16 2000 PATENT & TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

Docket No.: **1015-008**	Serial No.: **09/471,634**
	#4
Applicant: **Bryan D. Powell et al.**	
Application Filing Date: **December 24, 1999**	Group:

REFERENCE DESIGNATION **U. S. PATENT DOCUMENTS**

*Examiner Initial		Document Number	Date	Name	Class	Subclass
	1A	5,535,873	Jul 16, 1996	Sakamoto et al.	198	434
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

Duplicate of Paper #3

RECEIVED
NOV 22 2000
Technology Center 2100

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Name	Class	Subclass	Translation Yes	Translation No
	1L	WO 99 12406	11 Mar 1999	Matsushita	H05K	13/04	√- Abstract	
	1M	EP 1 018 862	12 Jul 2000	Matsushita	H05K	13/04		
	1N							
	1O							
	1P							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	1R	
	1S	
	1T	

Examiner Thomas Dickey Date Considered 11-5-02

*Examiner: Initial if citation is in conformance with MPEP 609; Draw line through

Notice of References Cited	Application/Control No. 09/471,675	Applicant(s)/Patent Under Reexamination ANDERSON ET AL.	
	Examiner Thomas Heckler	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,036,488	07-1991	Motarjemi	365/52
*	B	US-5,548,554	08-1996	Pascucci et al.	365/200
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

RECEIVED
MAY 21 2001
MIKIO ISHIMARU

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Washington, D.C. 20231

Serial Number: 09.471675

Filing Date: 12/24/99

Group Art Unit: 2182

Attorney Reference: 1015.003

STATUS LETTER REPLY

REQUESTER: Mikio Ishimaru

(✓) Attorney of Record

( ) Not of Record Therefore the following status information is being released to the following ATTORNEY OF RECORD: _____

( ) Not of Record - Unfortunately, the status information can not be released because the requestor is not of record. If this attorney should be of record, please forward additional changes to the Power of Attorney to the Customer Service Office.

STATUS INFORMATION

(✓) Action by the examiner
Expected date for action on this application
Mo. April Yr. 2002. Art unit 2182 is running 29 months for first action.

( ) Other (explain) _____

Sam Kim

Customer Service Office
Technology Center 2100
(703) 306-5631

PATENT APPLICATION ATTORNEY DOCKET NO. 1015-003

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: George Leland Anderson

Serial No.: 09/471,675 **Examiner:**

Filing Date: December 24, 1999 **Group Art Unit:**

Title: HIGH SPEED PROGRAMMER SYSTEM

COMMISSIONER FOR PATENTS
Washington D.C. 20231

STATUS INQUIRY

Sir:

1. More than 16 months have passed since:

   ☒ NEW APPLICATIONS
   the filing of this application on December 24, 1999. No communication has been received from the Patent and Trademark Office indicating action on this application.

   ☐ AMENDED APPLICATIONS
   the filing of a response on _____. No further communication has been received from the Patent and Trademark Office.

2. Kindly advise the undersigned of the present status of this application, by checking the appropriate box of the Status Inquiry Reply on the next page and returning it in the self-addressed envelope.

I hereby certify this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents
Washington, D.C. 20231.

Date of deposit: **May 3, 2001**

Signature: Tamara Tucker
Tamara Tucker

Respectfully submitted,

By Mikio Ishimaru
Mikio Ishimaru

Attorney/Agent for Applicant(s)
Reg. No. 27,449
Customer No.: 22898
Date: May 3, 2001

Telephone No.: 408 738-0592

MI/tt 107

Docket No.: 1015-003

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	George Leland Anderson et al. :		
Serial No.	09/471,675 :	Group Art Unit:	2787
Filed:	December 24, 1999 :	Examiner:	Unknown
For:	HIGH SPEED PROGRAMMER SYSTEM		

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL

Dear Sir:

Transmitted herewith is/are the following for the above-identified application:

- ☒ Information Disclosure Statement
- ☒ Form PTO-1449
- ☒ 3 Cited References:
- ☒ No additional fee is required
- ☐ Please charge my Deposit Account No. 50-0374 in the amount of $ 0.00. An additional copy of this transmittal sheet is submitted herewith.
- ☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 50-0374, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

Mikio Ishimaru

Mikio Ishimaru
Registration No. 27,449

The Law Offices of Mikio Ishimaru
1046 Pinenut Ct.
Sunnyvale, CA 94087
Tel: (408) 738-0592
Fax: (408) 738-0594
Date: November 4, 2000

Certificate of Mailing
I hereby certify that this correspondence is, on the date shown below, being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature Vickie Ishimaru
Vickie Ishimaru
Date 11/4/00

Docket No.: 1015-003 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	George Leland Anderson et al.	:	
Serial No.	09/471,675	:	Group Art Unit:
Filed:	December 24, 1999	:	Examiner:
For:	HIGH SPEED PROGRAMMER SYSTEM		

Assistant Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97, and 1.98 Applicants submit herewith patents, publications, or other information of which they are aware that they believe may be material to the examination of this application, and in respect of which, there may be a duty to disclose. The attention of the Patent and Trademark Office is hereby directed to the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed concurrently with the patent application, which is within three months of the U.S. filing date, or before the mailing date of a first Office Action on the merits. No certification or fee is required.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made (37 C.F.R. 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

The subject application is believed patentable over any of the references listed on the attached form.

Respectfully submitted,

Mikio Ishimaru

Mikio Ishimaru
Registration No. 27,449

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Date: November 4, 2000

FORM PTO-1449

Docket No.:	Serial No.:
1015-003	**09/471,675**

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

Applicant:	
George Leland Anderson et al.	
Application Filing Date: **December 24, 1999**	Group:

REFERENCE DESIGNATION **U. S. PATENT DOCUMENTS**

*Examiner Initial		Document Number	Date	Name	Class	Subclass
	1A	5,535,873	Jul 16, 1996	Sakamoto et al.	198	434
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Name	Class	Subclass	Translation	
							Yes	No
	1L	WO 99 12406	11 Mar 1999	Matsushita	H05K	13/04	√ - Abstract	
	1M	EP 1 018 862	12 Jul 2000	Matsushita	H05K	13/04		
	1N							
	1O							
	1P							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	1R	
	1S	
	1T	

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

PTO-103X
(Rev. 6-99)

FILING RECEIPT

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
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Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
09/471,675	12/24/99	2787	$608.00	1015-003	4	28	7

022898
THE LAW OFFICES OF MIKIO ISHIMARU
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SUNNYVALE CA 94807

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts of Application" ("Missing Parts Notice") in this application, please submit any corrections to this Filing Receipt with your reply to the "Missing Parts Notice." When the PTO processes the reply to the "Missing Parts Notice," the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s) GEORGE LELAND ANDERSON, BOTHELL, WA; ROBIN EDWARD CAMERON, SNOHOMISH, WA; SCOTT ALLEN FERN, KENT, WA.

CONTINUING DATA AS CLAIMED BY APPLICANT-
PROVISIONAL APPLICATION NO. 60/164,782 11/10/99

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 02/09/00 ** SMALL ENTITY **
TITLE
HIGH SPEED PROGRAMMER SYSTEM

PRELIMINARY CLASS: 713

DATA ENTRY BY: MOLLISH, CHRISTINE TEAM: 03 DATE: 02/09/00

Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	1015-003
First Inventor or Application Identifier	George Leland Anderson
Title	HIGH SPEED PROGRAMMER SYSTEM
Express Mail Label No.	EL413687907US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 22] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 4]
4. Oath or Declaration [*Total Pages* 2]
   - a. [X] Newly executed (original or copy)
   - b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [X] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: .....

16. If a **CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____

Prior application Information: *Examiner* _____ *Group / Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only: **The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.**

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 22898 *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

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Address					
City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	Mikio Ishimaru	*Registration No. (Attorney/Agent)*	27,449
Signature	Mikio Ishimaru	*Date*	Dec. 24, 1999

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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1. These are the fees effective October 1, 1997. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($ 648.00)

Complete if Known	
Application Number	
Filing Date	December 24, 1999
First Named Inventor	George Leland Anderson
Examiner Name	
Group / Art Unit	
Attorney Docket No.	1015-003

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 50-0374

Deposit Account Name: Mikio Ishimaru Law Offices

[X] Charge Any Additional Fee Required Under 37 C.F.R. § § 1.16 and 1.17

[ ] Charge the Issue Fee Set in 37 C.F.R. §1.18 at the Mailing of the Notice of Allowance

2. [ ] Payment Enclosed: [ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	380.00
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($ 380.00)

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	28	-20** = 8	X	9.00	= 72.00
Independent Claims	7	- 3** = 4	X	39.00	= 156.00
Multiple Dependent					= 0

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($ 228.00)

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	0.00
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	0.00
139	130	139	130	Non-English specification	0.00
147	2,520	147	2,520	For filing a request for reexamination	0.00
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	0.00
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	0.00
115	110	215	55	Extension for reply within first month	0.00
116	400	216	200	Extension for reply within second month	0.00
117	950	217	475	Extension for reply within third month	0.00
118	1,510	218	755	Extension for reply within fourth month	0.00
128	2,060	228	1,030	Extension for reply within fifth month	0.00
119	310	219	155	Notice of Appeal	0.00
120	310	220	155	Filing a brief in support of an appeal	0.00
121	270	221	135	Request for oral hearing	0.00
138	1,510	138	1,510	Petition to institute a public use proceeding	0.00
140	110	240	55	Petition to revive - unavoidable	0.00
141	1,320	241	660	Petition to revive - unintentional	0.00
142	1,320	242	660	Utility issue fee (or reissue)	0.00
143	450	243	225	Design issue fee	0.00
144	670	244	335	Plant issue fee	0.00
122	130	122	130	Petitions to the Commissioner	0.00
123	50	123	50	Petitions related to provisional applications	0.00
126	240	126	240	Submission of Information Disclosure Stmt	0.00
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	0.00
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	0.00
Other fee (specify) _____					0.00
Other fee (specify) _____					0.00

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($ 40.00)

SUBMITTED BY

				Complete (if applicable)	
Typed or Printed Name	Mikio Ishimaru			Reg. Number	27,449
Signature	Mikio Ishimaru	Date	12/24/99	Deposit Account User ID	

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HIGH SPEED PROGRAMMER SYSTEM

Docket Number: 1015-003

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HIGH SPEED PROGRAMMER SYSTEM

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application claims the benefit of U.S. Provisional Patent Application 60/164,782, filed on November 10, 1999, which is incorporated herein by reference thereto.

The present application contains subject matter related to a copending U.S. Patent Application by Lev M. Bolotin entitled "MANUFACTURING SYSTEM WITH FEEDER/PROGRAMMING/BUFFER SYSTEM". The related application is assigned to Data I/O Corporation, is identified by docket number 1015-001 and serial number 09/418,732, and is hereby incorporated by reference.

The present application contains subject matter related to a copending U.S. Patent Application by Bradley Morris Johnson, Lev M. Bolotin, Simon B. Johnson, Carl W. Olson, Bryan D. Powell, and Janine Whan-Tong entitled "FEEDER/PROGRAMMING/BUFFER OPERATING SYSTEM". The related application is assigned to Data I/O Corporation, is identified by docket number 1015-002 and serial number 09/419,172, and is hereby incorporated by reference.

The present application also contains subject matter related to a copending U.S. Patent Application by Simon B. Johnson, George Leland Anderson, Lev M. Bolotin, Bradley Morris Johnson, Mark Sean Knowles, Carl W. Olson, and Vincent Warhol entitled "FEEDER/PROGRAMMING/BUFFER CONTROL SYSTEM AND CONTROL METHOD". The related application is assigned to Data I/O Corporation, is identified by docket number 1015-004 and serial number 09/418,901, and is hereby incorporated by reference.

TECHNICAL FIELD

The present invention relates generally to a manufacturing system for electronic products, and more particularly to continuous production of electronic circuit boards incorporating programmable integrated circuits.

BACKGROUND ART

In the past, certain operations of electronic circuit board assembly were performed away from the main production assembly lines. While various feeder machines and robotic

handling systems would populate electronic circuit boards with integrated circuits, the operations related to processing integrated circuits, such as programming, testing, calibration, and measurement were performed in separate areas on separate equipment rather than being integrated into the main production assembly lines.

For example, in the programming of programmable devices such as electrically erasable programmable read-only memories (EEPROMs) and Flash EEPROMs, separate programming equipment was used which was often located in a separate area from the circuit board assembly lines. There were a number of reasons why programming was done off-line.

First, the programming equipment was relatively large and bulky. This was because of the need to accurately insert and remove programmable devices at high speeds into and out of programming sockets in the programmer. Since insertion and removal required relatively long traverses at high speed and very precise positioning, very rigid robotic handling equipment was required. This rigidity requirement meant that the various components had to be relatively massive with strong structural support members to maintain structural integrity and precision positioning of the pick and place system moving at high speeds. Due to the size of the programming equipment and the limited space for the even larger assembly equipment, they were located in different areas.

Second, a single high-speed production assembly system could use up programmed devices faster than they could be programmed on a single programming mechanism. This required a number of programmers which were generally operated for longer periods of time in order to have a reserve of programmed devices for the production assembly systems. This meant that the operating times and the input requirements were different between the two systems.

Third, no one had been able to build a single system which could be easily integrated with both the mechanical and electronic portions of the production assembly systems. These systems are complex and generally require a great deal of costly engineering time to make changes to incorporate additional equipment.

A major problem associated with programming the programmable devices in a separate area and then bringing the programmed devices into the production assembly area to be inserted into the electronic circuit boards was that it was difficult to have two separate processes running in different areas and to coordinate between the two separate systems. Often, the production assembly line would run out of programmable devices and the entire production assembly line would have to be shut down. At other times, the programming

that the production assembly line would not be shut down; however, this increased inventory costs. Further problems were created when the programming had to be changed and there was a large inventory of programmed integrated circuits on hand. In this situation, the inventory of programmable devices would have to be reprogrammed with an accompanying waste of time and money.

While it was apparent that a better system would be desirable, there appeared to be no way of truly improving the situation. There were a number of apparently insurmountable problems that stood in the way of improvement.

First, the operating speeds of current production assembly lines so greatly exceeded the programming speed capability of conventional programmers that the programmer would have to have a much greater throughput than thought to be possible with conventional systems.

Second, not only must the programmer be faster than existing programmers, it would also have to be much smaller. The ideal system would integrate into a production assembly line, but would do so without disturbing an existing production assembly line or requiring the lengthening of a new production assembly line over that of the length without the ideal system. Further, most of these production assembly lines were already filled with, or designed to be filled with, various types of feeding and handling modules which provide limited room for any additional equipment.

Third, any programmer tied into the production assembly line would have to also tie into the electronic feeders of the production assembly. This would require integration of any control software with the production system software for communication and scheduling purposes. This would be a problem because production assembly line system software was not only complex, but also confidential and/or proprietary to the manufacturers of those systems. This meant that the integration must be done with the cooperation of the manufacturers, who were reluctant to spend engineering effort on anything but improving their own systems, or must be done with a lot of engineering effort expended on understanding the manufacturers' software before working on the programmer's control software.

Fourth, the mechanical interface between a programmer and the production equipment needed to be highly accurate for placing programmed devices relative to the pick-and-place handling equipment of the production assembly system.

Fifth, there are a large number of different manufacturers of production handling equipment as well as production manufacturing equipment. This means that the a large number of different production assembly line configurations would have to be studied and major compromises in design required for different manufacturers.

Sixth, the ideal system would allow for changing quickly between different micro devices having different configurations and sizes.

Seventh, the ideal system needed to be able to accommodate a number of different micro device feeding mechanisms including tape, tape stacker, tube, tube stacker, and tape and reel.

Finally, there was a need to be able to quickly reject micro devices which failed during the programming.

All the above problems seem to render an effective solution impossible with the major problem being that the current state of this technology was such that it was not possible for programming equipment to keep up with the production line. Basically, it takes time to program an electronic device. A solution has been long sought for increasing the throughput of the integrated circuit programming systems.

DISCLOSURE OF THE INVENTION

The present invention provides a programmer system with significantly increased throughput. The system solves most of the problems previously occurring with the speed/throughput capability of conventional programmer systems while being optimized to provide efficient operation of the overall system.

The present invention provides a programmer system with a multiple number of sockets for programming a multiple number of micro devices simultaneously. Thus, the programming throughput can be increased significantly.

The present invention further provides a buffer circuit for a programmer system that is designed to program a number of different micro devices. The buffer circuit provides a plurality of logic levels suitable to drive different micro devices during programming.

The present invention further provides a method for programming a programmable micro device using a processor such that the processor address and data are used to supply the address and data required by the micro device. Instead of using a special bus cycle, the present invention uses the standard bus cycle from a processor for programming. Thus, the programming speed and the programming throughput are increased significantly.

The present invention still further provides a data compare circuit and a method for verifying data programmed by a programmer in a plurality of programmed micro devices using a single read-back operation. Thus, the programming speed and the programming throughput for a programmer that performs multi-device programming can be increased significantly.

The present invention further provides a processing mechanism which includes a processor for generating address signals, data signals and control signals; a pin driver module coupled to the processor; a backplane module coupled to the pin driver module; and at least one socket coupled to the backplane module. The at least one socket is used for placement of the unprocessed micro devices. The pin driver module routes the address signals, data signals and control signals to the backplane module, and provides a first plurality of voltages to the buffer circuit. The backplane module routes the address signals, data signals and control signals to the at least one socket, and provides a second plurality of voltages to the at least one socket. The programming mechanism substantially solves the throughput problem previously facing such systems.

The present invention further provides a buffer circuit for a processing mechanism capable of processing unprocessed micro devices into processed micro devices. The processing mechanism includes a processor for generating control data signals and processing data signals and for receiving device data signals; a voltage reference source for providing a voltage reference, and a V_{CCI} voltage supply for providing a V_{CCI} voltage; and at least one socket for placement of the unprocessed micro devices. The buffer circuit includes a digital-to-analog converter (DAC) coupled to the processor and the voltage reference source; an amplifier coupled to the DAC; and a level-shifting translating buffer coupled to the amplifer, the processor, the V_{CCI} voltage supply, and the socket for transferring processing data signals from the processor to the unprocessed micro devices and for transferring the device data signals from the processed micro devices to the processor. The DAC is responsive to the control data signals and the voltage reference to generate a first variable DC voltage. The amplifier is responsive to the first variable DC voltage to generate a second variable DC voltage. The level-shifting translating buffer is responsive to the V_{CCI} voltage and the second variable DC voltage for providing a plurality of logic levels for the device data signals. The buffer circuit substantially solves the throughput problem previously facing processing mechanism such as programmer systems.

The present invention further provides a method for programming a programmable micro device using a processor. The programmable micro device includes a plurality of memory locations for storing data. The memory locations are identified by a respective plurality of addresses. The programmable micro device is coupled to the processor via an address bus, a data bus and a control bus. The method includes the steps of: (a) providing a first address from the processor to the programmable micro device over the address bus; (b) providing a first data correpsonding to the first address from the processor to the programmable micro device over the data bus; and (c) providing a first control signal from the processor to the programmable micro device over the control bus to enable the programmable micro device to accept the first data from the processor at a memory location identified by the first address in the programmable micro device. The programming method substantially solves the throughput problem previously facing programmer systems.

The present invention further provides a programming mechanism capable of programming unprogrammed micro devices into programmed micro devices. The programmed micro devices having a plurality of memory locations for storing data. The plurality of memory locations is identified by a respective plurality of addresses. The programming mechanism includes a plurality of sockets for placement of processed micro devices; a plurality of data buffer/registers, wherein each of the plurality of data buffer/registers is coupled to a respective one of the plurality of sockets for receiving a first data stored in a first address in each of the programmed micro devices; a plurality of compare circuits, wherein each of the plurality of compare circuits has a first input and a second input and one output, and wherein the first input of each of the plurality of compare circuits is coupled to a respective one of the data buffer/registers for receiving the first data; an expected data register coupled to the second input of each of the respective plurality of compare circuits for providing a first expected data; a processor bus; and a processor coupled to the output of each of the plurality of compare circuits over the processor bus, wherein each of the compare circuits provides a first logic level at the output if the first data matches with the first expected data, and provides a second logic level at the output if the first data does not match with the first expected data. The programming mechanism substantially solves the throughput problem previously facing programmer systems.

The above and additional advantages of the present invention will become apparent to those skilled in the art from a reading of the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an overall block diagram of a programmer system of the present invention;

FIG. 2 is a schematic of the voltage level-shifing translating buffer of the present invention;

FIG. 3 is a schematic of the programmer system of the present invention in operation; and

FIG. 4 is a schematic of a portion of the programmer system of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Programming System:

The present invention provides a programmer system with multiple number of sockets for programming a multiple number of micro devices simultaneously. Thus the programming throughput can be increased significantly.

Referring now to FIG. 1, therein is shown a programmer system 10. The programmer system 10 includes a processor card 11 with a microprocessor, such as a processor 12 located thereon, a pin driver module 14, a backplane module 16, and a socket adapter 18 with four sockets 20A through 20D mounted thereon.

The processor 12 is coupled to the pin driver module 14 over an address bus 22 and a data/control bus 24. The processor 12 generates address, data, and control signals.

The pin driver module 14 includes a logic circuit 26 for routing the address, data, and control signals to the backplane module 16, and a voltage source circuit 28 for providing voltages to the backplane module 16. The logic circuit 26 may be a dedicated integrated circuit or a field programmable gate array (FPGA). The voltage source circuit 28 includes a conventional digital-to-analog converter (DAC) and conventional calibration circuits (not shown). The voltage source circuit 28 generates a V_{CC} supply voltage which is the normal operating supply voltage of the micro devices to be programmed and a programming voltage known as V_{PP}.

The backplane module 16 includes a plurality of relay switch circuits, four relay switch circuits 30A through 30D, and a plurality of buffer circuits, four buffer circuits 32A through 32D. The voltage source circuit 28 is coupled to the relay switch circuits/buffer circuits 30A/32A through 30D/32D over a power bus 34. The logic circuit 26 is coupled to each of the relay switch circuits/buffer circuits 30A/32A through 30D/32D over data/control

bus D/C0, D/C1, D/C2, and D/C3, respectively. The logic circuit 26 is also coupled to each of the relay switch circuits/buffer circuits 30A/32A through 30D/32D over an address bus 36.

The relay switch circuits/buffer circuits 30A/32A through 30D/32D are coupled to sockets 20A through 20B over busses 38A through 38D.

The backplane module 16 also controls status light-emitting diodes (LEDs) (not shown) for status of the sockets (20A through 20D) of a micro device that is being programmed. Status may indicate that the micro device is failing for some reason or that it is passing for some reason. It should be noted that the LEDs are optional in the practice of the present invention.

The socket adapter 18 is positioned over the backplane module 16 and has four sockets 20A through 20D for positioning the micro devices (not shown). One of the functions of the socket adapter 18 is to physically hold the micro devices in place while they are being programmed. The socket adapter 18 includes a ten-bit identification (ID) field so that it can be uniquely identified for the type of socket it carries, and therefore, the type of micro devices it may be able to hold. Since each interchangeable socket adapter 18 has a different type of socket depending on the manufacturer's device and package type, each socket adapter 18 needs to be uniquely identified using such an ID field.

In operation, the processor 12 first sets up the power and ground voltages for the micro devices to be programmed. To do that, the processor 12 provides control signals to the relay switch circuits 30A through 30D, via the logic circuit 26. This will set up the proper relay configuration such that power and ground are properly routed to each micro device and each socket 20A through 20D. Once power and ground are set up correctly, the processor 12 writes to the voltage source circuit 28 over the data/control bus 24 and sets the proper voltage levels for the micro device that needs to be programmed. These voltage levels would include the V_{CC} supply for the micro device, the V_{PP} supply which is also known as the programming supply voltage, and a third voltage V_{IH} which is the voltage of the signals that are used to drive the micro device while it is programmed.

The logic circuit 26 provides the address and data from the address bus 22 and the data/control bus 24 directly to each micro device that is being programmed in each socket 20A through 20D. This arrangement makes this interface to appear as though the micro device is part of the processor card 11 and that it is directly connected to the address and data bus of the processor 12 and can be directly written to.

For different types of micro devices, different requirements exist for the number of address lines and/or the number of data lines needed to be accessed during each bus cycle. To accommodate different types of micro devices, the logic circuit 26 is capable of sizing each bus for each micro device to match the size of the micro device that is to be programmed.

Once the micro devices are considered part of the processor 12 bus and can be written to directly, a programming algorithm as stated by the micro device manufacturer will be followed to give the correct command sequence to the micro devices in order to program them. For a multi-socket design such as in this embodiment (four-socket design), the data to be written from the processor 12 to a micro device is sent simultaneously to the other three micro devices such that all four micro devices are programmed simultaneously.

Thus, a multiple number of micro devices can be programmed simultaneously using a programmer system constructed in accordance with the present invention. Therefore, the programming throughput can be increased significantly.

It would be evident to those skilled in the art that modifications could be made to allow micro devices in the sockets to be programmed in random order. This would be desirable when it is desired to keep the sockets as full as possible and the programming operations on-going as much as possible. As a micro device is programmed or found to be defective, it would be replaced and programing would start immediately.

Voltage Level-Shifting Translating Buffers

The present invention provides a buffer circuit for a programmer system that is designed to program a number of different micro devices. The buffer circuit provides a plurality of logic levels suitable to drive different types of micro devices during programming.

Referring to FIG.2, therein is shown a buffer circuit 60 for a programmer system, such as the programmer system 10, of FIG. 1. The buffer circuit 60 includes a digital-to-analog converter (DAC) 62, an amplifier 64, a calibration circuit 66, and a level-shifting translating buffer 68. The DAC 62 includes a read/write (W/R) terminal coupled to a processor, such as the processor 12 of FIG. 1, via line 70, a V_{REF} terminal coupled to a reference voltage source (not shown) via conductive line 72. The DAC 62 is also coupled to the processor 12 for receiving control data signals therefrom over a data bus 74.

The amplifier 64 includes a resistor 76 having a first terminal coupled to the output of the DAC 62, a capacitor 78 having a first terminal coupled to a second terminal of the resistor 76 and a second terminal coupled to ground 80, an operational amplifier 82 having its positive terminal coupled to the first terminal of the capacitor 78 and its output terminal coupled to its negative terminal.

The calibration circuit 66 includes an operational amplifier 84 having its positive terminal coupled to the output terminal of the amplifier 64, its negative terminal coupled to a precision voltage reference via line 86 and its output terminal coupled to a first terminal of a resistor 88 and a calibration roll back via line 90. The second terminal of the resistor 88 is coupled to +5V.

The level-shifting translating buffer 68 includes a latch 92, a V_{CC1} terminal coupled to +5V, a V_{CC2} terminal coupled to the output terminal of the amplifier 64, the second terminal coupled to ground 80, a read/write direction (DIR) terminal, and an output enable (OE) terminal. The level-shifting translating buffer 68 is coupled to the processor 12 for transferrring programming data over a bus 94 to the unprocessed micro devices, and coupled to the micro devices for transfering device data over a bus 96 to the processor 12.

In operation, the processor 12 sends control data signals to the DAC 62 over the data bus 74. The DAC 62 then generates a first variable DC voltage based on the control data signals and the voltage reference V_{REF}. This voltage reference V_{REF} defines the full-scale range of voltage that the DAC 62 can put out. For example, if a voltage reference V_{REF} equals 10 volts, the DAC 62 has the capability of outputting voltages ranging from zero to 10 volts. In response to the first variable DC voltage, the amplifier 64 generates a second variable DC voltage. The second variable DC voltage is then provided to the level-shifting translating buffer 68.

The second variable DC voltage is used as a power source for the level-shifting translating buffer 68. V_{CC1} is connected to a constant voltage supply and is used to interface the programming data from the processor 12 to its appropriate voltage level, in this case 5 volts. V_{CC2}, which is coupled to the second variable DC voltage, is used to control the bus 96 going out to the micro device. Since the second variable DC voltage controls the output level to the bus 96, the bus 96 is able to support 1.5-volt to 5-volt logic micro devices.

In this embodiment, the level-shifting translating buffer 68 is used to transfer the data from the processor 12 to the micro devices. With this particular configuration, the data coming from the processor 12 is always known to be of a certain logic level, i.e., whatever

the processor 12 is designed to use. For a 5-volt logic on the processor 12 side, the level-shifting translating buffer 68 then translates the 5-volt logic levels to whatever the voltage that's applied to the V_{CC2} terminal of the level-shifting translating buffer 68.

Thus, a buffer circuit for a programmer system can be formed in acccordance with the present invention to provide a plurality of logic levels suitable to drive micro devices with different voltage requirement during programming.

Direct-Write Programming

The present invention provides a method for programming a programmable micro device using a processor such that the processor address and data are used to supply the address and data required by the micro device. Instead of using a special bus cycle, the present invention uses the standard bus cycle from a processor for programming. Therefore, the programming speed and the programming throughput are increased significantly.

Referring to FIG.3, therein is shown a processor, such as the processor 12, connected to a programmable micro device, such as a Flash memory device 112, via an address bus 114, a data bus 116, and a control bus 118. A V_{PP} switch 120 is shown coupled between the processor 12 and a V_{PP} terminal of the Flash memory device 112. The Flash memory device 112 includes a plurality of memory locations for storing data (not shown). The memory location is identified by a respective plurality of addresses (not shown). The memory locations and identifications are characteristics of such devices.

The memory address location that will be written or read to by the processor 12 will be sent over the address bus 114. The data bus 116 carries the data from the processor 12 to the Flash memory device 112. The data bus 116 is bi-directional in that the processor 12 can write this data to the Flash memory device 112 or the Flash memory device 112 can output the data for the processor 12 to read.

The control bus 118 carries the control signals from the processor 12 to the Flash memory device 112 for generating chip-enable, write-enable, and output-enable signals. These signals control when the Flash memory device 112 is going to program and when it's going to output data for read operations.

In operation, the processor 12 sends out a valid address to the Flash memory device over the address bus 114, along with valid data that it wants to write over the data bus 116. The processor 12 ensures that the chip-enable of the Flash memory device 112 is in an active

state which is typically low; and then sends the write-enable pulse to the Flash memory device 112 over the control bus 118.

The high-to-low transition on the write-enable pulse, which is on the control bus 118, will start the programming operation inside the Flash memory device 112. At that time the processor 12 must go back to a specific address. After the programming operation has started, the processor 12 will typically put out a specific address and poll the data until specific data that is defined in the programming specification is read back on the data lines.

By checking the data that is returned on the data bus 116 and comparing it with the data sent by the processor 12 over the data bus 116, the processor 12 can determine whether the programming has been performed successfully. If the data sent by the processor 12 is different from the data that is read back, the Flash memory device 112 have not been programmed successfully. The Flash memory device 112 may be programmed again and then go through the same data comparison again. The programming, followed by the data comparison, can be repeated for a predetermined number (N) of times before the Flash memory device 112 is considered to be a reject. When this happens, the processor 12 will provide a signal, such as turning on an LED or sounding an alarm, to indicate a programming failure. This is repeated throughout the entire address space, or at least the block of data that is required to be programmed into the Flash memory device 112. Once this operation is completed, the device is considered programmed.

Further operations usually require a verification to ensure that the Flash memory device 112 was properly programmed. In which case, the processor 12 will go back to wherever it has stored its expected data and then repeat the earlier process of putting out each address, reading back the data, and comparing it against the data that it intended to write into the Flash memory device 112. This would validate that the programming operation did indeed happen correctly and that the Flash memory device 112 was properly programmed.

When the V_{PP} switch is used for older memory devices that require a special programming voltage, the V_{PP} switch would be inactive or turned off during the read-back, or verification mode.

Thus, by using the standard bus cycle from a processor for programming a micro device using the processor in accordance with the present invention, the programming speed and the programming throughput can be increased significantly.

GANG-DATA COMPARE

The present invention provides a data compare circuit and a method for verifying data programmed by a programmer in a plurality of programmed micro devices using a single read-back operation. Thus the programming speed and the programming throughput for a programmer that performs multi-device programming can be increased significantly.

Referring to FIG.4, therein is shown a programmer 140 constructed in accordance with the present invention which is capable of programming unprogrammed micro devices into programmed micro devices. The programmer 140 includes four sockets (142A through 142D) for placement of processed micro devices (not shown); four data buffer/registers (144A through 144D) coupled to the four sockets (142A through 142D) over data busses 146A through 146D, respectively, for receiving data stored in a first adress in each of the four processed micro devices; four compare circuits (148A through 148D), an expected data register 152, a processor bus 156 and the processor 12 coupled to the processor bus 156. In this embodiment, the compare circuits include exclusive OR gates.

Each of the four data buffer/registers 144A through 144D is coupled to a first terminal of a respective one of the compare circuits 148A through 148D over data busses 150A through 150D, respectively. The expected data buffer/register 152 is coupled to a second terminal of each of the compare circuits 148A through 148D. The output terminals of the compare circuits 148A through 148D are coupled to the processor bus 156 via lines 154A through 154D, respectively.

To begin the verification process (data compare or read-back operation), the four data buffer/registers 144A through 144D presents the data being read from the four micro devices (not shown) inserted in sockets 142A through 142D. The data comes from a first address in each of the micro devices during the read operation. The output of the latched data in each of the data buffer/registers 144A through 144D is then compared with the expected data provided by the expected data register 152 using the compare circuits 148A through 148D. In this embodiment, each of the compare circuits 148A through 148D includes an exclusive OR gate. The output of each of the compare circuits 148A through 148D will be at a first logic level if the data from the micro device matches the expected data from the expected data register 152. Otherwise, the output will be at a second logic level. The output of each of the compare circuits 148A through 148D is then put out as a bit (represented by either the first logic level or the second logic level) to the processor bus 156 over each of the lines 154A through 154D. The processor 12 reads back the output of the each of the compare

circuits 148A through 148D over microprocessor bus 156 as part of the read cycle for this read operation.

The logic levels represented by the four bits coming out of the compare circuits 148A through 148D identify the micro device that failed the compare operation. If there is no failure, the verification can be allowed to continue with the next address. If there is a failure, the data from sockets 142A through 142D can be read directly out of the data buffer/registers 144A through 144D. The expected data can be read from the expected data register 152. A comparison can then be made by the processor 12 to determine which bits of the data had failed.

When a micro device failed the data compare operation, it may be considered as a reject. Alternatively, a micro device that failed the data compare operation may be reprogrammed for a number of times before it is considered a reject.

It should be noted that the width of the data busses 150A through 150D is the same the width as a regular data bus for the micro devices. For example, if the micro device is a 16-bit device, then each of the data busses 150A through 150D will be 16-bits wide. Therefore, the compare circuits 148A through 148D compares sixteen data lines, with a single output indicating that those sixteen lines passed or failed.

Thus, the data compare circuits and method according to the present invention verify data programmed by a programmer in a plurality of programmed micro devices by using a single read-back operation. Thus the programming speed and the programming throughput for a programmer that performs multi-device programming can be increased significantly.

From the above it will be understood that the present invention is applicable to what can be described as "micro devices". Micro devices include a broad range of electronic and mechanical devices. The best mode describes processing which is programming for programmable devices, which include but are not limited to devices such as Flash memories (Flash), electrically erasable programmable read only memories (E^2PROM), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), and microcontrollers. However, the present invention encompasses processing for all electronic, mechanical, hybrid, and other devices which require testing, measurement of device characteristics, calibration, and other processing operations. For example, these types of micro devices would include but not be limited to devices such as microprocessors, integrated circuits (ICs), application specific integrated circuits (ASICs), micro mechanical machines, micro-electro-mechanical (MEMs) devices, micro modules, and fluidic systems.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations which fall within the spirit and scope of the included claims. All matters set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

THE INVENTION CLAIMED IS:

1. A processing mechanism for processing unprocessed micro devices into processed micro devices, comprising:

a processor for generating address signals, data signals and control signals;

a pin driver module coupled to the processor;

a backplane module coupled to the pin driver module; and

at least one socket coupled to the backplane module, the at least one socket for placement of the unprocessed micro devices; wherein:

the pin driver module routes the address signals, data signals and control signals to the backplane module, and provides a first plurality of voltages to the backplane module;

the backplane module routes the address signals, data signals and control signals to the at least one socket, and provides a second plurality of voltages to the at least one socket.

2. The processing mechanism as claimed in claim 1 wherein:

the pin driver module includes:

a logic circuit for routing the address signals, data signals and control signals to the backplane module, and

a voltage source circuit for providing the first plurality of voltages to the buffer circuit.

3. The processing mechanism as claimed in claim 1 wherein:

the backplane module includes:

a relay switch circuit for routing the address signals, data signals and control signals to the at least one socket, and

a buffer circuit for providing the second plurality of voltages to the at least one socket.

4. The processing mechanism as claimed in claim 2 wherein the logic circuit includes a field programmable gate array.

5. The processing mechanism as claimed in claim 2 wherein the voltage source circuit includes a digital to analog converter.

6. The processing mechanism as claimed in claim 2 wherein the first plurality of voltages includes a V_{CC} voltage and a processing voltage for processing the unprocessed micro devices.

7. The processing mechanism as claimed in claim 2 wherein the first plurality of voltages includes a V_{pp} voltage and a processing voltage for processing the unprocessed micro devices.

8. A processing mechanism for processing unprocessed micro devices into processed micro devices, comprising:

a processor for generating address signals, data signals and control signals;

a pin driver module coupled to the processor, the pin driver module including a logic circuit and a voltage sources circuit;

a backplane module coupled to the pin driver module, the backplane module including a relay switch circuit and a buffer circuit; and

at least one socket coupled to the backplane module, the at least one socket for placement of the unprocessed micro devices; wherein:

the logic circuit routes the address signals, data signals and control signals to the backplane module, and the voltage source circuit provides a first plurality of voltages to the buffer circuit;

the relay switch circuit routes the address signals, data signals and control signals to the at least one socket, and the buffer circuit provides a second plurality of voltages to the at least one socket.

9. The processing mechanism as claimed in claim 8 wherein the logic circuit includes a field programmable gate array.

10. The processing mechanism as claimed in claim 8 wherein the voltage source circuit includes a digital-to analog converter.

11. The processing mechanism as claimed in claim 8 wherein the first plurality of voltages includes a V_{CC} voltage and a processing voltage for processing the unprocessed micro devices.

12. The processing mechanism as claimed in claim 8 wherein the first plurality of voltages includes a V_{pp} voltage and a processing voltage for processing the unprocessed micro devices.

13. A buffer circuit for a processing mechanism capable of processing unprocessed micro devices into processed micro devices, the processing mechanism having a processor for generating control data signals and processing data signals and for receiving device data signals, a voltage reference source for providing a voltage reference, and a V_{CC1} voltage supply for providing a V_{CC1} voltage, and at least one socket for placement of the

unprocessed micro devices, the programming data signals are of V_{CC1} volt logic levels, comprising:

a digital-to-analog converter (DAC) coupled to the processor and the voltage reference source, the DAC responsive to the control data signals and the voltage reference to generate a first variable DC voltage;

an amplifier coupled to the DAC, the amplifier responsive to the first variable DC voltage to generate a second variable DC voltage; and

a level-shifting translating buffer coupled to the amplifer, the processor, the V_{CC1} voltage supply, and the socket for transferring processing data signals from the processor to the unprocessed micro devices and for transferring the device data signals from the processed micro devices to the processor, the level-shifting translating buffer responsive to the V_{CC1} voltage and the second variable DC voltage to provide a plurality of logic levels for the device data signals.

14. The buffer circuit as claimed in claim 13 wherein the first variable voltage has a value between 0 volt and the voltage reference.

15. The buffer circuit as claimed in claim 13 wherein the amplifier is an operational amplifier.

16. The buffer circuit as claimed in claim 13 wherein the plurality of logic levels is between 0 volts and V_{CC1} volts.

17. A method for programming a programmable micro device using a processor, the programmable micro device having a plurality of memory locations for storing data, the memory locations being identified by a respective plurality of addresses, the programmable micro device being coupled to the processor via an address bus, a data bus and a control bus, comprising the steps of:

(a) providing a first address from the processor to the programmable micro device over the address bus;

(b) providing a first data corresponding to the first address from the processor to the programmable micro device over the data bus; and

(c) providing a first control signal from the processor to the programmable micro device over the control bus to enable the programmable micro device to accept the first data from the processor at a memory location identified by the first address in the programmable micro device.

18. The method as claimed in claim 17 including the steps of:

(d) providing a second control signal from the processor to the programmable micro device over the control bus to enable the programmable micro device to provide to the processor data stored in the memory location identified by the first address over the data bus; and

(e) comparing the data stored in the memory location identified by the first address in the programmable micro device with the first data.

19. The method as claimed in claim 18 including the steps of:

(f) repeating steps (a) through (e) when the data stored in the memory location identified by the first address in the programmable micro device is not identical to the first data.

20. The method as claimed in claim 19 including the steps of:

(g) providing a signal by the processor to indicate a programming failure when, after repeating steps (a) through (e) for a predetermined number (N) of times, the data stored in the memory location identified by the first address in the programmable micro device is still not identical to the first data, wherein N is an integer.

21. A method for reading a programmable micro device using a processor, the programmable micro device having a plurality of memory locations for storing data, the memory locations being identified by a respective plurality of addresses, the programmable micro device being coupled to the processor via an address bus, a data bus and a control bus, comprising the steps of:

(a) providing a first address from the processor to the programmable micro device over the address bus; and

(b) providing a first control signal from the processor to the programmable micro device over the control bus to enable the programmable micro device to provide a first data from a memory location identified by the first address in the programmable micro device over the data bus.

22. A programming mechanism capable of programming unprogrammed micro devices into programmed micro devices, the programmed micro devices having a plurality of memory locations for storing data, the plurality of memory locations being identified by a respective plurality of addresses, comprising:

a plurality of sockets for placement of processed micro devices;

a plurality of data buffer/registers, each of the plurality of data buffer/registers coupled to a respective one of the plurality of sockets for receiving a first data stored in a first address in each of the programmed micro devices;

a plurality of compare circuits, each of the plurality of compare circuits having a first input and a second input and one output, the first input of each of the plurality of compare circuits being coupled to a respective one of the data buffer/registers for receiving the first data;

an expected data register coupled to the second input of each of the respective plurality of compare circuits for providing a first expected data;

a processor bus; and

a processor coupled to output of each of the plurality of compare circuits over the processor bus, wherein each of the compare circuits provides a first logic level at the output when the first data matches with the first expected data, and provides a second logic level at the output when the first data does not match with the first expected data.

23. The programming mechanism as claimed in claim 22 wherein the compare circuits are exclusive OR gates.

24. A method for verifying data programmed in a plurality of programmed micro devices using a programming mechanism capable of programming unprogrammed micro devices into programmed micro devices, the programmed micro devices having a plurality of memory locations for storing data, the plurality of memory locations being identified by a respective plurality of addresses, comprising steps of:

(a) providing to each of a plurality of data buffer/registers a first data stored in a first address in each of the plurality of programmed micro devices;

(b) providing the first data to a first input of each of a plurality of compare circuits;

(c) providing a first expected data from an expected data register to a second input of each of the plurality of compare circuits;

(d) comparing the first data with the first expected data using the plurality of compare circuits;

(e) outputting a first logic level at an output of a respective one of the plurality of compare circuits when the first data matches with the first expected data, and

(f) outputting a second logic level at the output of a respective one of the plurality of compare circuits when the first data does not match with the first expected data.

25. The method as claimed in claim 24 including the steps of:

(g) identifying, after step (f), the programmed micro devices that include the first data which does not match with the first expected data by detecting a logic level at the output of the plurality of compare circuits.

26. The method as claimed in claim 25 including the steps of:

(h) programming, after step (g), the programmed micro devices when the programmed micro devices include the first data which does not match with the first expected data.

27. The method as claimed in claim 25 including the steps of:

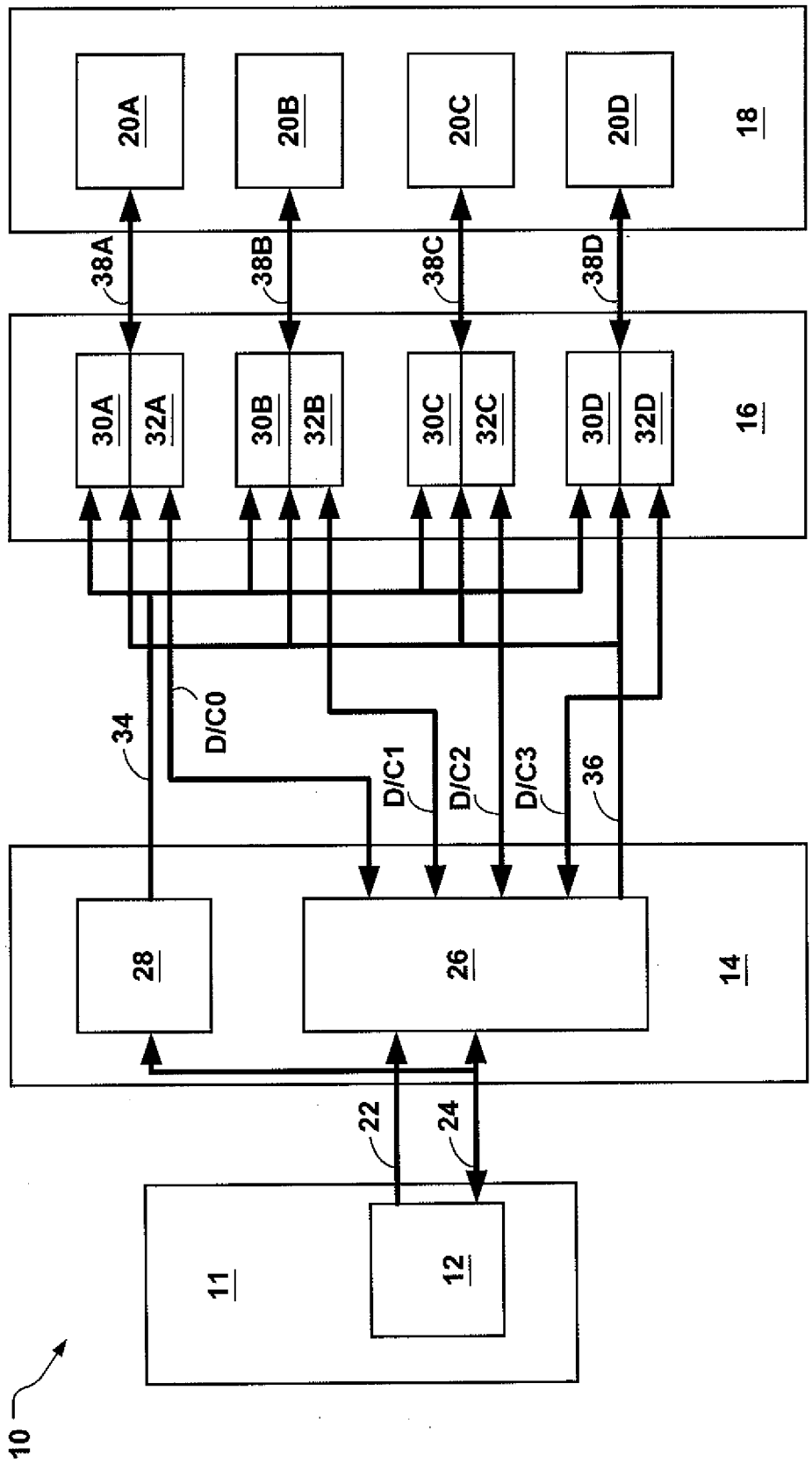
(i) rejecting, after step (g), the programmed micro devices when the programmed micro devices include the first data which does not match with the first expected data.

28. The method as claimed in claim 25 including the steps of:

(j) repeating steps (a) to (f) for a second data stored in a second address in each of the plurality of programmed micro devices.

ABSTRACT

A programmer system and method of programming programmable micro devices with significantly increased throughput are provided. The programmer system includes a multiple number of sockets for programming a multiple number of micro devices simultaneously. A buffer circuit is also provided which is capable of providing a number of logic levels suitable to drive different micro devices during programming by a programmer system adapted to program a number of micro devices simultaneously. A method for programming a programmable micro device is further provided which uses the standard bus cycle from a processor for programming. Finally, a data compare circuit and a method for verifying data programmed by a programmer in a plurality of programmed micro devices using a single read-back operation is also disclosed.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D/C2
D/C3

FIG. 1

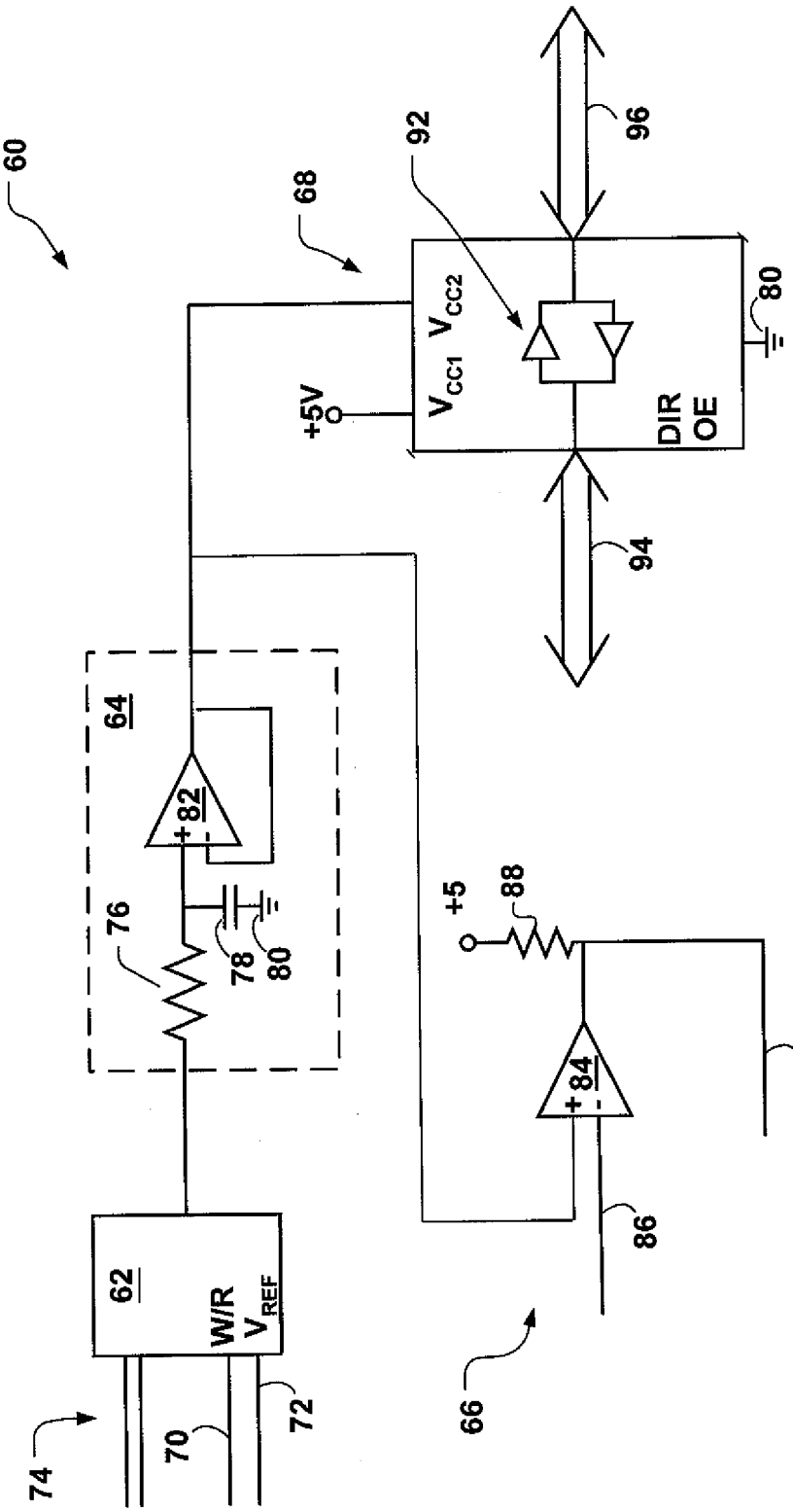
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FIG. 2

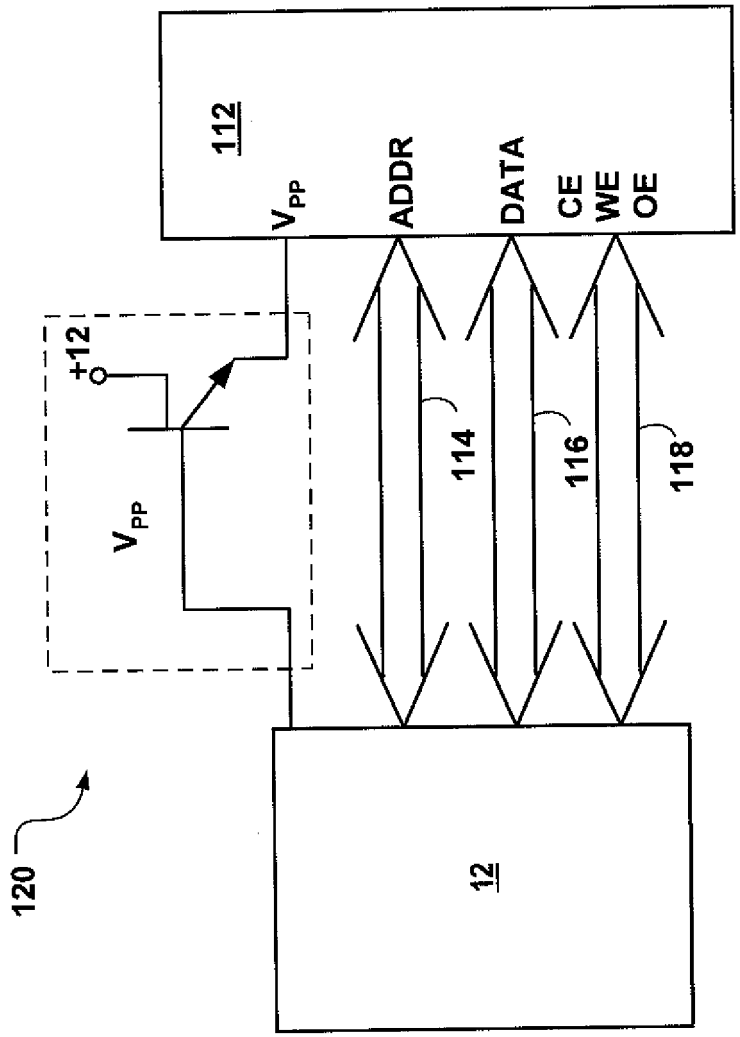
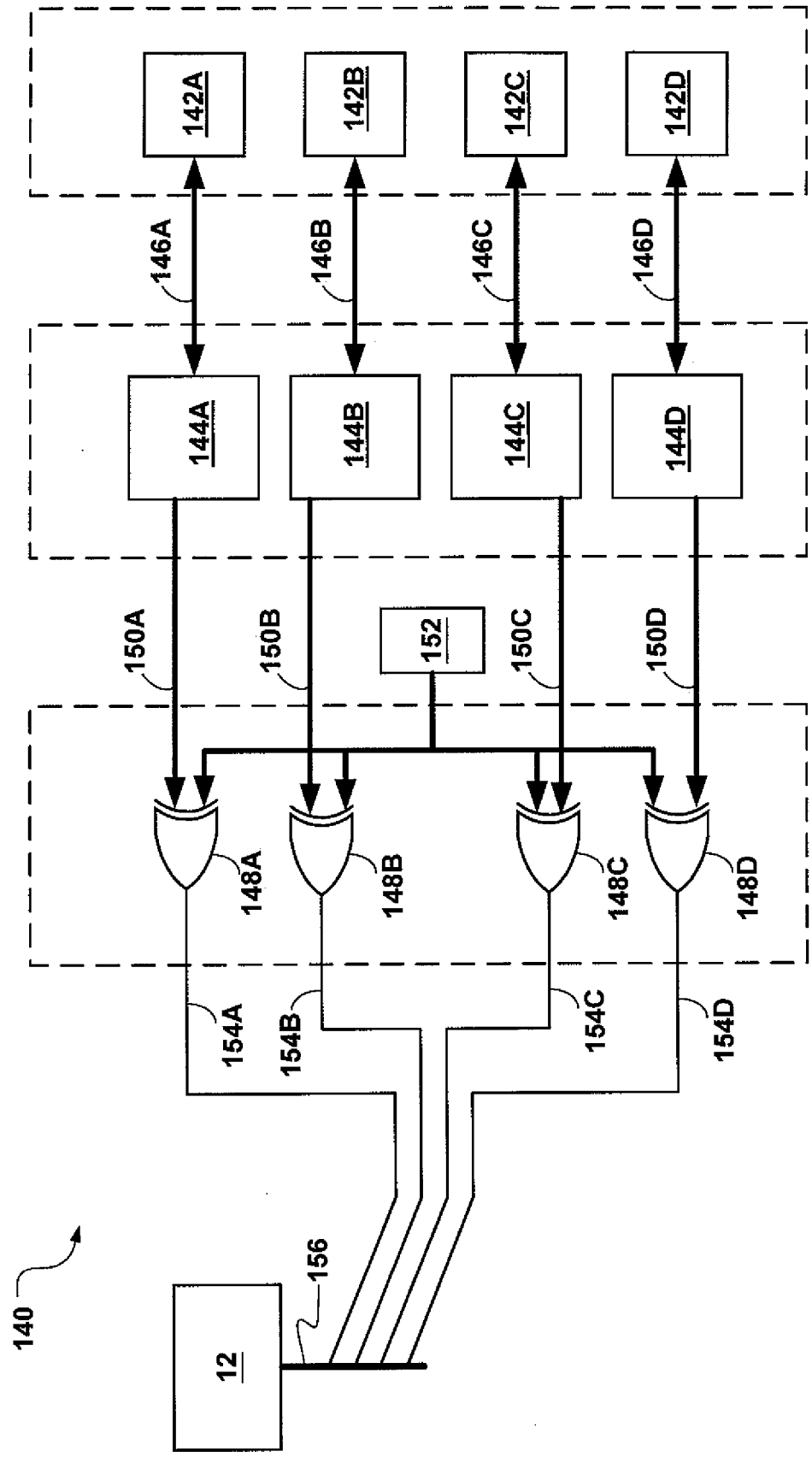


FIG. 3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152
150C
150D
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FIG. 4

Docket No.: 1015-003 *PATENT*
Express Mail Label No.: EL413687907US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	George Leland Anderson et al.	:	
Serial No.		:	Group Art Unit:
Filed:	Dec. 24, 1999	:	Examiner:
For:	HIGH SPEED PROGRAMMER SYSTEM		

Assistant Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97, and 1.98 Applicants submit herewith patents, publications, or other information of which they are aware that they believe may be material to the examination of this application, and in respect of which, there may be a duty to disclose. The attention of the Patent and Trademark Office is hereby directed to the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed concurrently with the patent application, which is within three months of the U.S. filing date or before the mailing date of a first Office Action on the merits. No certification or fee is required.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made (37 C.F.R. 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

The subject application is believed patentable over any of the references listed on the attached form.

The relevance of each non-English language reference, if any, is discussed in the present specification.

Respectfully submitted,

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December 24, 1999

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FORM PTO-1449

Docket No.:	Serial No.:
1015-003	
Applicant: George Leland Anderson et al.	
Filing Date: December 24, 1999	Group:

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

REFERENCE DESIGNATION **U. S. PATENT DOCUMENTS**

*Examiner Initial		Document Number	Date	Name	Class	Subclass
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	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

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		Document Number	Date	Name	Class	Subclass	Translation Yes	Translation No
	1L							
	1M							
	1N							
	1O							
	1P							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	1R	BP-6500 In-Line Programming System brochure, BP Microsystems, Inc. 1999, 2 pages.
	1S	BP-6500 In-Line Programming System Data Sheet, BP Microsystems, Inc. 1999, 1 page.
	1T	"BP-6500 In-Line Programming & Fifth Generation Technology", BP Microsystems, Inc. 1999, 7 pages.

Examiner	Date Considered

FORM PTO-1595
(Rev. 6-93)
OMB No. 0651-0011 (exp. 4/94)

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Robin Edward Cameron

Scott Allen Fern

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):

Name: DATA I/O CORPORATION

Internal Address: _____

Street Address: 10525 Willows Road N.E.

City: Redmond State: WA ZIP: 98052

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:

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Execution Date: December 23, 1999 (by all 3 Assignors)

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If this document is being filed together with a new application, the execution date of the application is: 12/23/1999

A. Patent Application No.(s)

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☒ No

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7. Total fee (37 CFR 3.41) ..... $ 40.00

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Name of Person Signing	Signature	Date

Total number of pages including cover sheet, attachments, and document: 4

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patents & Trademarks, Box Assignments
Washington, D.C. 20231

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
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NOTICE OF ALLOWANCE AND FEE(S) DUE

22898 7590 11/06/2002

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

MIKIO ISHIMARU

NOV 12 2002

RECEIVED

EXAMINER	
HECKLER, THOMAS M	
ART UNIT	CLASS-SUBCLASS
2185	713-001000

DATE MAILED: 11/06/2002

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

TITLE OF INVENTION: HIGH SPEED PROGRAMMER SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$640	$0	$640	02/06/2003

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Box ISSUE FEE
Commissioner for Patents
Washington, D.C. 20231
Fax (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

22898 7590 11/06/2002

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

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nonprovisional	YES	$640	$0	$640	02/06/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
HECKLER, THOMAS M	2185	713-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) ❑ individual ❑ corporation or other private group entity ❑ government

4a. The following fee(s) are enclosed:

❑ Issue Fee

❑ Publication Fee

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s):

❑ A check in the amount of the fee(s) is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date)

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SUITE A1
SUNNYVALE, CA 94087
UNITED STATES

EXAMINER	
HECKLER, THOMAS M	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/06/2002

Determination of Patent Term Extension under 35 U.S.C. 154 (b)

(application filed after June 7, 1995 but prior to May 29, 2000)

The patent term extension is 0 days. Any patent to issue from the above identified application will include an indication of the 0 day extension on the front page.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date that determines patent term extension is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system. (http://pair.uspto.gov)

Any questions regarding the patent term extension or adjustment determination should be directed to the Office of Patent Legal Administration at (703)305-1383.

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,675	12/24/1999	GEORGE LELAND ANDERSON	1015-003	7801

22898 7590 11/06/2002

THE LAW OFFICES OF MIKIO ISHIMARU
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SUNNYVALE, CA 94087
UNITED STATES

EXAMINER	
HECKLER, THOMAS M	
ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/06/2002

Notice of Possible Fee Increase on October 1, 2002

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2002, then the amount due may be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there may be an increase in fees effective on October 1, 2002. See Revision of Patent and Trademark Fees for Fiscal Year 2003; Notice of Proposed Rulemaking, 67 Fed. Reg. 30634, 30636 (May 7, 2002). Although a change to the amount of the publication fee is not currently proposed for October 2002, if the issue fee or publication fee is to be paid on or after October 1, 2002, applicant should check the USPTO web site for the current fees before submitting the payment. The USPTO Internet address for the fee schedule is: http://www.uspto.gov/main/howtofees.htm.

If the issue fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due," but not the correct amount in view of any fee increase, a "Notice to Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice to Pay Balance of Issue Fee," if the response to the Notice of Allowance and Fee(s) due form is to be filed on or after October 1, 2002 (or mailed with a certificate of mailing on or after October 1, 2002), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability	Application No.	Applicant(s)	
	09/471,675	ANDERSON ET AL.	
	Examiner	Art Unit	
	Thomas Heckler	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
2. ☒ The allowed claim(s) is/are *1-28*.
3. ☒ The drawings filed on *24 December 1999* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☒ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☒ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____ .
5☒ Information Disclosure Statements (PTO-1449), Paper No. *2-4*.
6☒ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other

Thomas Heckler
Primary Examiner
Art Unit: 2185

1. The following changes to the drawings are required by the examiner: labels are required for the boxes of Figs. 1, 3, 4 as per 37 C.F.R. 1.83(a). In order to avoid abandonment of the application, applicant must make these drawing changes.

2. The following is an examiner's statement of reasons for allowance: the prior art does not teach a processing mechanism for processing unprocessed micro devices into processed micro devices comprising a pin driver module for routing address, data and control signals to a backplane module and provide a first plurality of voltages to the backplane module, the backplane module routing the address, data and control signals and providing a second plurality of voltages to at least one socket wherein the unprocessed micro device is placed;

nor does the prior art teach a buffer circuit for a processing mechanism capable of processing unprocessed micro devices into processed micro devices comprising a digital-to-analog converter to generate a first variable DC voltage, an amplifier responsive to the DC voltage to generate a second variable DC voltage, and a level-shifting translating buffer for transferring data signals from a processor to the unprocessed micro devices and for transferring the device data signals from the processed micro devices to the processor, the buffer responsive to a voltage and the second variable DC voltage to provide a plurality of logic levels for the device data signals;

nor does the prior art teach a method for programming a programmable micro device comprising providing a first address from a processor, providing a first data corresponding to the

first address, and providing a control signal to enable the micro device to accept the data at a memory location identified by the first address;

nor does the prior art teach a method for reading a programmable micro device comprising providing a first address from a processor to the micro device and providing a control signal from the processor to the micro device to enable the device to provide a first data from a memory location identified by the first address;

nor does the prior art teach a programming mechanism capable of programming unprogrammed micro devices into programmed micro devices comprising a plurality of sockets for placement of processed micro devices, a plurality of data buffer/registers, each coupled to a socket for receiving a first data, a plurality of compare circuits having one input coupled to a respective buffer/register, an expected data register coupled to the second input of a respective compare circuit, and a processor coupled to the output of each of the plurality of compare circuits, wherein each compare circuit provides a first logic level when the first data matches the first expected data, and provides a second logic level when the first data does not match the first expected data;

nor does the prior art teach a method for verifying data programmed in a plurality of programmed micro devices comprising providing to each of a plurality of data buffer/registers a first data stored in each of the plurality of programmed micro devices, providing the first data to a first input of a plurality of compare circuits, providing a first expected data from an expected data register to a second input of each of the plurality of compare circuits, comparing the first data

with the first expected data, outputting a first logic level from one of the compare circuits when the first data matches with the first expected data, and outputting a second logic level from one of the compare circuits when the first data does not match with the first expected data.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom Heckler whose telephone number is (703) 305-9666.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (703) 305-3900.

THOMAS M. HECKLER
PRIMARY EXAMINER

TH
November 5, 2002

FORM PTO-1449

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

Docket No.:	Serial No.:
1015-003	09/471,675
Applicant: **George Leland Anderson et al.**	
Filing Date: **December 24, 1999**	Group: 2185

REFERENCE DESIGNATION **U. S. PATENT DOCUMENTS**

*Examiner Initial		Document Number	Date	Name	Class	Subclass
	1A					
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Name	Class	Subclass	Translation	
							Yes	No
	1L							
	1M							
	1N							
	1O							
	1P							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

JKH	1R	BP-6500 In-Line Programming System brochure, BP Microsystems, Inc. 1999, 2 pages.
JKH	1S	BP-6500 In-Line Programming System Data Sheet, BP Microsystems, Inc. 1999, 1 page.
JKH	1T	"BP-6500 In-Line Programming & Fifth Generation Technology", BP Microsystems, Inc. 1999, 7 pages.

Examiner Thomas Lee Date Considered 11-5-02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

FORM PTO-1449

Docket No.:	Serial No.:
1015-003	**09/471,675**

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

Applicant:	
George Leland Anderson et al.	
Application Filing Date: **December 24, 1999**	Group: 2185

REFERENCE DESIGNATION **U. S. PATENT DOCUMENTS**

*Examiner Initial		Document Number	Date	Name	Class	Subclass
	1A	5,535,873	Jul 16, 1996	Sakamoto et al.	198	434
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Name	Class	Subclass	Translation Yes	Translation No
	1L	WO 99 12406	11 Mar 1999	Matsushita	H05K	13/04	√ - Abstract	
	1M	EP 1 018 862	12 Jul 2000	Matsushita	H05K	13/04		
	1N							
	1O							
	1P							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

1R	
1S	
1T	

Examiner [signature] Date Considered 11-5-02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through

FORM PTO-1449

OIPE
NOV 16 2000
PATENT & TRADEMARK OFFICE

Docket No.: 1015-008	Serial No.: 09/471,634
	#4
Applicant: Bryan D. Powell et al.	
Application Filing Date: December 24, 1999	Group:

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

U. S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass
	1A	5,535,873	Jul 16, 1996	Sakamoto et al.	198	434
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

duplicate of paper #3

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Technology Center 2100

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Name	Class	Subclass	Translation Yes	Translation No
	1L	WO 99 12406	11 Mar 1999	Matsushita	H05K	13/04	√ - Abstract	
	1M	EP 1 018 862	12 Jul 2000	Matsushita	H05K	13/04		
	1N							
	1O							
	1P							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

1R	
1S	
1T	

Examiner Thomas Dickey Date Considered 11-5-02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

Notice of References Cited

Application/Control No.	Applicant(s)/Patent Under Reexamination	
09/471,675	ANDERSON ET AL.	
Examiner	Art Unit	Page 1 of 1
Thomas Heckler	2185	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,036,488	07-1991	Motarjemi	365/52
*	B	US-5,548,554	08-1996	Pascucci et al.	365/200
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.